厦门IC设计公共服务平台管理中心

培 训 通 知

各集成电路相关企业：

厦门 IC 平台联合 Cadence 工程师于 2018 年 01 月 17 日在厦门 IC 平台会议室开展 Quantus QRC 相关培训。主要介绍以下三个方面：Overview and Technology Setup、Parasitic Extraction 、Extracted View Flows and Advanced Features。

详细的培训内容如下：

时间	2018 年 01 月 17 日 9:00-17:00（8 课时）
地点	厦门集成电路设计公共服务平台 厦门软件园二期观日路 34 号之一 101 会议室
培训内容	➢ The T1 course is designed to offer user-level experience on the next generation parasitic extraction solution from Cadence®–Quantus QRC. You explore the documentation system and Cadence online support. You will learn the parasitic extraction challenges in design closure and Quantus QRC solutions to tackle it. You will also see how Quantus QRC extraction fits into the design flow and how to set up the extraction environment. You will analyze Quantus-QRC technology directory structure, explore extraction features and check out modes – GUI and command-line – of effectively extracting parasitic resistance, capacitance and inductance. ➢ The T2 course is designed to offer user-level experience on the next generation parasitic extraction solution from Cadence®–Quantus QRC. You explore the documentation system and Cadence® online support. You start with an overview of the PVS–Quantus QRC data flow and advance to hands-on extraction activities. You then set up the extraction environment in GUI mode or command line. You explore the considerations, settings and various features for Quantus parasitic extraction such as random walk field solver, adaptive meshing, split wide MOS or hierarchical extraction and then run multi-corner extraction with Quantus and perform Reduction Control & Advanced Virtual Metal Fill (VMF). Under specific extraction capabilities, you check out parasitic inductance extraction with PEEC -- Wide

	Band Models and parasitic substrate extraction with Substrate Noise Analysis (SNA). ➢ The T3 course is designed to offer user-level experience on the next generation parasitic extraction solution from Cadence®--Quantus QRC. You first explore the documentation system and Cadence® online support and then explore the advanced node design solutions in Quantus QRC. You will analyze extraction challenges in FINFETs, 3DIC and Double Patterning (DPT) designs and respective Quantus QRC solutions. You will also learn how the extracted viewis integrated into the Virtuoso environment. You explore the Virtuoso® Parasitic Aware Designer (VPAD) flow, Parasitic Resimulation Flow and analog post-layout simulation flow in detail. Finally, you set up and perform EMIR analysis on Spectre/APS/MMSIM simulators in ADE environment.
参会对象	各 IC 设计企业技术人员

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二〇一八年一月二日